

IN THE CLAIMS

1. (Currently Amended) A semiconductor memory device having a first access mode and a second access mode and including comprising:

a plurality of word lines; comprising:

an arbiter which receives configured to receive a first entry signal for entering [[the]] a first access mode and a second entry signal for entering [[the]] a second access mode, and determines to determine priority of the first and second access modes in accordance with an order of receipt of the first and second entry signals, and sequentially generates, and to generate a first mode trigger signal corresponding to [[the]] a first entry mode signal and a second mode trigger signal corresponding to [[the]] a second entry mode signal in accordance with the determined priority; and

a signal generating circuit, connected to the arbiter, for generating configured to generate an internal operation signal in accordance with at least one of the first mode trigger signal and the second mode trigger signal, wherein the arbiter executes the first access mode by priority over the second access mode, when the arbiter is supplied with the first entry signal within a predetermined period after priority for the second access mode has been determined,

wherein the predetermined period comprises a period from a point at which the second entry signal is enabled to a point at which a predetermined word line of the plurality of word lines is enabled in the second access mode gives priority to the first access mode when the arbiter receives the first entry signal during the time after the second entry signal is supplied and before a predetermined word line of the plurality of word lines is enabled in the second access mode.

2. (Currently Amended) The semiconductor ~~memory~~ device according to claim 1, wherein the arbiter determines whether the first entry signal has been supplied within [[the]] a predetermined period or not in accordance with the internal operation signal.

3. (Currently Amended) The semiconductor ~~memory~~ device according to claim [[2]] 1, wherein

the internal operation signal is used as a decision signal indicating whether or not a predetermined word line is enabled in the second access mode.

4. (Currently Amended) The semiconductor ~~memory~~ device according to claim [[2]] 1, wherein

~~the internal operation signal includes the signal generating circuit generates~~ a word-line enable signal for enabling [[a]] the predetermined word line in the second access mode.

5. (Currently Amended) The semiconductor ~~memory~~ device according to claim 4, further comprising an address generating circuit, ~~connected to the signal generating circuit, for generating that generates~~ an address to be used in the second access mode in accordance with the word-line enable signal.

6. (Original) The semiconductor ~~memory~~ device according to claim 5, wherein the arbiter generates a state signal indicative of the second access mode in accordance with the second entry signal, and

the address generating circuit generates the address in accordance with the state signal and the word-line enable signal.

7. (Currently Amended) The semiconductor ~~memory~~ device according to claim 1, wherein the arbiter includes:

a first decision circuit which receives the first entry signal and the second entry signal and determines priority of the first and second access modes ~~in accordance with the order of receipt of the first and second entry signals,~~

~~a second decision circuit, connected to the first decision circuit, for determining that determines whether the first entry signal has been supplied within the predetermined period or not, and~~

~~a mode trigger generating circuit, connected to the first decision circuit, for generating that generates the first mode trigger signal in accordance with the determined priority, and~~

wherein the mode trigger generating circuit generates the first mode trigger signal when the first entry signal is supplied to the second decision circuit within the predetermined period.

8. (Currently Amended) The semiconductor ~~memory~~ device according to claim 7, wherein the second decision circuit generates a cancel signal ~~for stopping to stop~~ execution of the second access mode when the first entry signal is supplied within the predetermined period.

9. (Currently Amended) The semiconductor ~~memory~~ device according to claim 8, wherein after generating the cancel signal, the second decision circuit generates the second entry signal again to execute the second access mode after execution of the first access mode.

10. (Currently Amended) The semiconductor ~~memory~~ device according to claim 1, further including an address generating circuit ~~for generating that generates~~ an address to be used for the second access mode, and

wherein the address generating circuit does not generate the address when the arbiter determines the first access mode has priority.

11. (Currently Amended) The semiconductor ~~memory~~ device according to claim 1, wherein the arbiter includes a time setting unit ~~which~~ that determines whether the first entry signal has been supplied within the predetermined period or not.

12. (Currently Amended) The semiconductor ~~memory~~ device according to claim 1, ~~wherein the device has a test mode and further comprises comprising~~ an exclusive test terminal ~~to which~~ that supplies the second entry signal ~~for the~~ in a test mode is supplied.

13. (Currently Amended) The semiconductor ~~memory~~ device according to claim 12, wherein

the internal operation signal includes a word-line enable signal ~~for enabling to~~ enable a predetermined word line in the second access mode, and

the signal generating circuit suppresses generation of the word-line enable signal in accordance with a test signal.

14. (Currently Amended) The semiconductor ~~memory~~ device according to claim 12, wherein in the test mode, the signal generating circuit receives the first entry signal and generates the word-line enable signal.

15. (Currently Amended) The semiconductor ~~memory~~ device according to claim 1, wherein the device has a test mode and further comprises an external terminal to which the second entry signal for the test mode is supplied.

16. (Currently Amended) The semiconductor memory device according to claim 1, wherein the first access mode [[is]] corresponds to a read or write operation mode and the second access mode [[is]] corresponds to a self-refresh operation mode.

17. (Currently Amended) The semiconductor memory device according to claim 1, wherein

the internal operation signal includes a word-line enable signal for enabling a predetermined word line in the second access mode, and

the predetermined period comprises a period from a point at which the second entry signal is enabled prior to enabling of the first entry signal to a point at which the word-line enable signal is enabled.

18. (Currently Amended) A semiconductor memory device having a first access mode and a second access mode and including comprising:

a plurality of word lines, comprising: and

an arbiter which receives configured to receive a first entry signal for entering [[the]] a first access mode and a second entry signal for entering [[the]] a second access mode, and determines to determine priority of the first and second access modes in accordance with an order of receipt of the first and second entry signals, and to generate a first mode trigger signal corresponding to a first entry mode and a second mode trigger signal corresponding to a second entry mode,

whereby in case of receiving the first entry signal within a predetermined period after having received the second entry signal, the arbiter stops executing the second access mode and executes the first access mode,

~~wherein the predetermined period comprises a period from a point at which the second entry signal is enabled to a point at which a predetermined word line of the plurality of word lines is enabled in the second access mode wherein the arbiter gives priority to the first access mode when the arbiter receives the first entry signal during the time after the second entry signal is supplied and before a predetermined word line of the plurality of word lines is enabled in the second access mode.~~

19. (Currently Amended) The semiconductor ~~memory~~ device according to claim 18, further comprising a signal generating circuit, connected to the arbiter, for generating configured to generate an internal operation signal in accordance with at least one of a first mode trigger signal corresponding to the first entry signal and a second mode trigger signal corresponding to the second entry signal, and
~~wherein the predetermined time is a time at which the internal operation signal is generated.~~

20. (Currently Amended) The semiconductor ~~memory~~ device according to claim 19, wherein

the internal operation signal includes a word-line enable signal for enabling a predetermined word line in the second access mode.

21. (Currently Amended) A method for controlling a semiconductor memory device having a first access mode and a second access mode, the method and ~~including a plurality of word lines~~, comprising ~~the steps of~~:

determining priority of the first and second access modes in accordance with a first entry signal for entering the first access mode and a second entry signal for entering the second access mode;

executing the second access mode when the second access mode is determined to have priority;

detecting if the first entry signal has been supplied within a predetermined period after execution of the second access mode has been started and before a predetermined word line of a plurality of word lines is enabled in the second access mode; and

executing the first access mode by priority over the second access mode when the first entry signal is detected;

~~wherein the predetermined period comprises a period from a point at which execution of the second access mode was started to a point at which a predetermined word line in the semiconductor memory device is enabled in the second access mode.~~

22. (Original) The method according to claim 21, wherein the step of executing the first access mode includes stopping execution of the second access mode.

23. (Original) The method according to claim 22, further comprising the step of executing the second access mode after the stopping, and execution of the first access mode.

24. (Currently Amended) The method according to claim 22, further comprising the step of stopping generation of an address of [[a]] the predetermined word line for the second access mode of the semiconductor memory device if the stopping of execution of the second access mode is performed.

25. (Currently Amended) The method according to claim 21, wherein the first access mode [[is]] corresponds to a read or write operation mode ~~requested by an~~

external unit, and the second access mode [[is]] corresponds to a self-refresh operation mode for refreshing data inside the semiconductor memory device, and the first access mode and the second access mode are executed asynchronously relative to each other.

26. (Original) The method according to claim 21, wherein the predetermined period comprises a period from a point at which execution of the second access mode was started to a point at which a predetermined word line in the semiconductor memory device is enabled in the second access mode.

27. (Original) The method according to claim 26, further comprising the step of setting in the second access mode, a word line address for executing a next second access mode after the predetermined word line is enabled.

28. (Original) The method according to claim 21, wherein the predetermined period comprises a period from a point at which the second access mode was executed to a point at which a word-line enable signal is generated for enabling a predetermined word line in the semiconductor memory device in the second access mode.

29. (Currently Amended) A method for testing access time in manufacturing a semiconductor memory device having a first access mode and a second access mode and including a plurality of word lines, the method comprising the steps of:

supplying a second entry signal for entering [[the]] a second access mode to the semiconductor memory device and executing the second access mode;

supplying a first entry signal for entering [[the]] a first access mode to the semiconductor memory device within a predetermined period after supplying the second entry signal;

enabling a predetermined word line in the semiconductor memory device in accordance with the first entry signal in the second access mode;

executing the ~~second~~ first access mode after the first access mode is finished; and

measuring a period from a point at which the first entry signal is supplied to a point at which the first access mode is finished;

~~wherein the predetermined period comprises a period from a point at which the second entry signal is enabled to a point at which a predetermined word line of the plurality of word lines is enabled in the second access mode.~~

30. (Original) The method according to claim 29, wherein the semiconductor memory device has a normal mode to perform a normal operation and a test mode for conducting a test, further comprising the step of switching from the normal mode to the test mode when the second entry signal is supplied.

31. (New) A semiconductor device comprising:

a plurality of word lines;
an arbiter configured to receive a first entry signal for entering a first access mode and a second entry signal for entering a second access mode, to determine priority of the first and second access modes, and to generate a first mode trigger signal corresponding to a first entry mode and a second mode trigger signal corresponding to a second entry mode; and

a signal generating circuit configured to generate an internal operation signal in accordance with at least one of the first mode trigger signal and the second mode trigger signal,

wherein the arbiter interrupts the second access mode and gives priority to the first access mode when the arbiter receives the first entry signal before a predetermined word line of the plurality of word lines is enabled in the second access mode and after priority for the second access mode has been determined.

Claim 32. (New) A semiconductor device comprising:

an arbiter configured to receive a first entry signal for entering a first access mode and a second entry signal for entering a second access mode, to determine priority of the first and second access modes, and to generate a first mode trigger signal corresponding to a first entry mode and a second mode trigger signal corresponding to a second entry mode; and

a signal generating circuit configured to generate an internal operation signal in accordance with at least one of the first mode trigger signal and the second mode trigger signal,

an address generating circuit configured to generate an address to be used in the second access mode,

wherein the arbiter gives priority to the first access mode when the arbiter receives the first entry signal before the address generating circuit generates the address to be used in the second access mode and after priority for the second access mode has been determined.

Claim 33. (New) The semiconductor device according to claim 1, further comprising a command detector circuit that receives an external command and generates the first entry signal.

Claim 34. (New) The semiconductor device according to claim 1, further comprising an internal circuit that generates the second entry signal.

Claim 35 (New) The semiconductor device according to claim 1, wherein the first access mode corresponds to an external access operation and the second access mode corresponds to an internal access operation.

Claim 36. (New) The semiconductor device according to claim 32, further comprising a command detector circuit that receives an external command and generates the first entry signal.

Claim 37. (New) The semiconductor device according to claim 32, further comprising an internal circuit that generates the second entry signal.

Claim 38. (New) The semiconductor device according to claim 32, wherein the first access mode corresponds to an external access operation and the second access mode corresponds to an internal access operation.

Claim 39. (New) The semiconductor device according to claim 19, wherein the predetermined time is a time when the internal operation signal is generated.

Claim 40. (New) The semiconductor device according to claim 21, wherein the first access mode corresponds to an external access operation and the second access mode corresponds to an internal access operation.